What Is Claimed Is:

1. A digital system that performs a specified basic function by operating a plurality of mutually interdependent flip-flops to perform digital processing according to one or more clock signals, comprising:

a plurality of delay elements which are inserted respectively in a plurality of clock circuits that supply said clock signals in said digital system and each of which is composed of a circuit element that changes a delay time according to a value indicated by a control signal, and

a plurality of holding circuits that hold a plurality of control signals to be given to said plurality of delay elements, wherein;

said plurality of control signals having values that are changed by an external device, by (i) inputting a test signal to said digital system and observing a resultant output of the digital system and a resulting operational environment of the digital system, (ii) evaluating a fitness of the digital system from the observed output and operational environment of the digital system, and (iii) using a probabilistic search technique based on said evaluated fitness of the digital system, so that said basic function of the digital system satisfies a predetermined specification.

2. A digital system according to claim 1, wherein the values of the control signals held by said holding circuits are changed to optimum values for bringing said digital system into a state where said basic function of the digital system satisfies the predetermined specification, said optimum values being values which said external device has searched by changing in order the values of said control signals according to a genetic algorithm.

3. A digital system according to claim 1, wherein said plurality of control signals are changed by said external device while raising the frequency of said clock signal in stages.

4. A digital system according to claim 1, wherein said digital system is composed as an integrated circuit.

5. A digital system according to claim 1, wherein said digital system is composed as a circuit board.

6. A digital system according to claim 1, wherein said operational environment of the digital system is a parameter that can be physically observed.

7. A digital system according to claim 6, wherein said parameter is a current consumption amount of the digital system.

8. A digital system according to claim 6, wherein said parameter is a power of electromagnetic wave dissipated from the digital system.

9. A digital system that performs a specified basic function by operating a plurality of mutually interdependent flip-flops to perform digital processing according to one or more clock signals, comprising:

a plurality of delay elements which are inserted respectively in a plurality of clock circuits that supply said clock signals in said digital system and each of which is composed of a circuit element that changes a delay time according to a value indicated by a control signal,

a plurality of holding circuits that hold a plurality of control signals to be given to said plurality of delay circuits, and

a setting means that changes the values of said plurality of control signals by (i) inputting a test signal to said digital system and observing a resultant output of the digital system and a resulting operational environment of the digital system, (ii) evaluating a fitness of the digital system from the observed output and operational environment of the digital system, and (iii) using a probabilistic search technique based on said evaluated fitness of the digital system, so that said basic function of the digital system satisfies a predetermined specification.

10. A digital system according to claim 9, wherein said setting means changes in order the values of said control signals according to a genetic algorithm and searches optimum values of said control signals for bringing said digital system into a state where said basic function of the digital system satisfies the predetermined specification.

11. A digital system according to claim 9, wherein said plurality of control signals are changed by said setting means while raising the frequency of said clock signal in stages.

12. A digital system according to claim 9, wherein said digital system is composed as an integrated circuit.

13. A digital system according to claim 9, wherein said digital system is composed as a circuit board.

14. A digital system according to claim 9, wherein said operational environment of the digital system is a parameter that can be physically observed.

15. A digital system according to claim 14, wherein said parameter is a current consumption amount of the digital system.

16. A digital system according to claim 14, wherein said parameter is a power of electromagnetic wave dissipated from the digital system.

17. A method for adjusting timing of one or more clock signals of a digital system that performs a specified basic function by operating a plurality of mutually interdependent flip-flops to perform digital processing according to said clock signals, said method comprising the steps of:

inserting a plurality of delay elements respectively in a plurality of clock circuits that supply said clock signals in said digital system,

forming said plurality of delay elements respectively out of circuit elements each changing a delay time according to a value indicated by a control signal,

holding a plurality of control signals to be given to said plurality of delay elements in a plurality of holding circuits provided in said digital system, and

changing the values of said plurality of control signals by an external device, by (i) inputting a test signal to said digital system and observing a resultant output of the digital system and a resulting operational environment of the digital system, (ii) evaluating a fitness of the digital system from the observed output and operational environment of the digital system, and (iii) using a probabilistic search technique based on said evaluated fitness of the digital system, so that said basic function of the digital system satisfies a predetermined specification.

18. A method for adjusting a clock signal of a digital system according to claim 17, wherein said external device changes in order the values of said control signals according to a genetic algorithm and searches optimum values of said control

signals for bringing said digital system into a state where said basic function of the digital system satisfies the predetermined specification.

19. A method for adjusting a clock signal of a digital system according to claim 17, wherein changing said plurality of control signals by said external device is performed while raising the frequency of said clock signal in stages.

20. A method for adjusting a clock signal of a digital system according to claim 17, wherein said digital system is composed as an integrated circuit.

21. A method for adjusting a clock signal of a digital system according to claim 17, wherein said digital system is composed as a circuit board.

22. A method for adjusting a clock signal of a digital system according to claim 17, wherein said operational environment of the digital system is a parameter that can be physically observed.

23. A method for adjusting a clock signal of a digital system according to claim 22, wherein said parameter is a current consumption amount of the digital system.

24. A method for adjusting a clock signal of a digital system according to claim 22, wherein said parameter is a power of electromagnetic wave dissipated from the digital system.

25. A method for adjusting a clock signal of a digital system according to claim 17, wherein said external device is composed of an electronic computer.

26. A recording medium on which is recorded a processing program that is executed by said electronic computer in a method for adjusting a clock signal of a digital system according to claim 17, and changes the values of said plurality of control signals held by said plurality of holding circuits according to a probabilistic search technique so that said basic function of the digital system satisfies the predetermined specification.

27. A method for adjusting timing of a one or more clock signals of a digital system that performs a specified basic function by operating a plurality of mutually interdependent flip-flops to perform digital processing according to said clock signals, said method comprising the steps of:

inserting a plurality of delay elements respectively in a plurality of clock circuits that supply said clock signals in said digital system,

forming said plurality of delay elements respectively out of circuit elements each changing a delay time according to a value indicated by a control signal,

holding a plurality of control signals to be given to said plurality of delay elements in a plurality of holding circuits provided in said digital system, and

changing the values of said plurality of control signals by a setting means provided in said digital system, by (i) inputting a test signal to said digital system and observing a resultant output of the digital system and a resulting operational environment of the digital system, (ii) evaluating a fitness of the digital system from the observed output and operational environment of the digital system, and (iii) using a probabilistic search technique based on said evaluated fitness of the digital system, so that said basic function of the digital system satisfies a predetermined specification.

28. A method for adjusting a clock signal of a digital system according to claim 27, wherein said setting means changes in order the values of said control signals according to a genetic algorithm and searches optimum values of said control signals for bringing said digital system into a state where said basic function of the digital system satisfies the predetermined specification.

29. A method for adjusting a clock signal of a digital system according to claim 27, wherein said plurality of control signals are changed by said setting means while raising the frequency of said clock signal in stages.

30. A method for adjusting a clock signal of a digital system according to claim 27, wherein said digital system is composed as an integrated circuit.

31. A method for adjusting a clock signal of a digital system according to claim 27, wherein said digital system is composed as a circuit board.

32. A method for adjusting a clock signal of a digital system according to claim 27, wherein said operational environment of the digital system is a parameter that can be physically observed.

33. A method for adjusting a clock signal of a digital system according to

claim 32, wherein said parameter is a current consumption amount of the digital system.

34. A method for adjusting a clock signal of a digital system according to claim 32, wherein said parameter is a power of electromagnetic wave dissipated from the digital system.

35. A method for adjusting a clock signal of a digital system according to claim 27, wherein said setting means is composed of an electronic computer.

36. A recording medium on which is recorded a processing program that is executed by said electronic computer in a method for adjusting a clock signal of a digital system according to claim 27, and changes the values of said plurality of control signals held by said plurality of holding circuits according to a probabilistic search technique so that said basic function of the digital system satisfies the predetermined specification.